Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device having a surface, comprising:

a plurality of conductive sub-surface regions of a first conductivity each formed beneath a well comprising a channel ~~said surface~~ of said semiconductor and each buried at a depth below said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure; and

at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said sub-surface structure via a plurality of tap contacts.

2. (Original) The semiconductor device as recited in Claim 1 wherein said sub-surface structure is a diagonal sub-surface mesh structure.

3-5. (Canceled)

6. (Original) The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has an N-type doping.

7. (Original) The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a P-type doping.

8. (Original) The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a strip shape.

9. (Original) The semiconductor device as recited in Claim 1 wherein said metal structure has a metal wire shape.

10. (Original) The semiconductor device as recited in Claim 1 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

11. (Currently Amended) A semiconductor device having a surface, comprising:

a first plurality of conductive sub-surface regions of a first conductivity each formed beneath a well comprising a channel ~~said surface~~ of said semiconductor and each buried at a depth below said surface, wherein said first plurality of conductive sub-surface regions form a first sub-surface structure for routing a body-bias voltage;

a second plurality of conductive sub-surface regions of said first conductivity each formed beneath said surface and each buried at a depth below said surface, wherein said second plurality of conductive sub-surface regions form a second sub-surface structure for routing said body-bias voltage;

an isolation structure formed between said first sub-surface structure and said second sub-surface structure such that said isolation structure creates a gap between said first sub-surface structure and said second sub-surface structure; and

at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said first sub-surface structure and said second sub-surface structure via a plurality of tap contacts.

12. (Original) The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first diagonal sub-surface mesh structure, and wherein said second sub-surface structure is a second diagonal sub-surface mesh structure.

13-15. (Canceled)

16. (Original) The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has an N-type doping.

17. (Original) The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a P-type doping.

18. (Original) The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a strip shape.

19. (Original) The semiconductor device as recited in Claim 11 wherein said metal structure has a metal wire shape.

20. (Original) The semiconductor device as recited in Claim 11 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said first and second sub-surface structures, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

21. (Currently Amended) A semiconductor device having a surface, comprising:

a plurality of conductive sub-surface regions of a first conductivity each formed beneath a well comprising a channel ~~said surface~~ of said semiconductor and each buried at a depth below said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure; and

at least one structure that spans said gap and is coupled to said sub-surface structure.

22. (Original) The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface mesh structure.

23-25. (Canceled)

26. (Original) The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has an N-type doping.

27. (Original) The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a P-type doping.

28. (Original) The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a strip shape.

29. (Original) The semiconductor device as recited in Claim 21 wherein said structure is a polysilicon wire.

30. (Original) The semiconductor device as recited in Claim 21 wherein said structure is a diffusion wire.

31. (Original) The semiconductor device as recited in Claim 21 wherein said structure is a silicide wire.

32. (Original) The semiconductor device as recited in Claim 21 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

33. (Original) The semiconductor device as recited in Claim 21 wherein said isolation structure divides said sub-surface structure into a first portion and a second portion.

34. (Previously Presented) The semiconductor device as recited in Claim 1, wherein a pattern of said plurality of conductive sub-surface regions is selected based on resistance characteristics of a conductive path for routing said body-bias voltage.

35. (Previously Presented) The semiconductor device as recited in Claim 34, wherein said pattern is selected to prevent isolation of wells of said semiconductor device.

36. (Previously Presented) The semiconductor device as recited in Claim 1, wherein a pattern, location and size of said plurality of conductive sub-surface regions is selected based on the distribution of wells of said semiconductor device.

37. (Previously Presented) The semiconductor device as recited in Claim 1, wherein said isolation structure creates a gap that separates said conductive sub-surface regions to at least two regions.

38. (Previously Presented) The semiconductor device as recited in Claim 1, wherein said isolation structure creates a gap that interrupts said conductive sub-surface regions.

39. (Previously Presented) The semiconductor device as recited in Claim 11, wherein a pattern of said first and said second plurality of conductive sub-surface regions are selected based on resistance characteristics of a conductive path for routing said body-bias voltage.

40. (Previously Presented) The semiconductor device as recited in Claim 39, wherein said pattern is selected to prevent isolation of wells of said semiconductor device.

41. (Previously Presented) The semiconductor device as recited in Claim 11, wherein a pattern, location and size of said plurality of conductive sub-surface regions is selected based on the distribution of wells of said semiconductor device.

42. (Previously Presented) The semiconductor device as recited in Claim 11, wherein said isolation structure creates a gap that separates said conductive sub-surface regions to at least two regions.

43. (Previously Presented) The semiconductor device as recited in Claim 11, wherein said isolation structure creates a gap that interrupts said conductive sub-surface regions.

44. (Previously Presented) The semiconductor device as recited in Claim 21, wherein a pattern of said plurality of conductive sub-surface regions is selected based on resistance characteristics of a conductive path for routing said body-bias voltage.

45. (Previously Presented) The semiconductor device as recited in Claim 44, wherein said pattern is selected to prevent isolation of wells of said semiconductor device.

46. (Previously Presented) The semiconductor device as recited in Claim 21, wherein a pattern, location and size of said plurality of conductive sub-surface regions is selected based on the distribution of wells of said semiconductor device.

47. (Previously Presented) The semiconductor device as recited in Claim 21, wherein said isolation structure creates a gap that separates said conductive sub-surface regions to at least two regions.

48. (Previously Presented) The semiconductor device as recited in Claim 21, wherein said isolation structure creates a gap that interrupts said conductive sub-surface regions.